PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Terunao HANAOKA

Group Art Unit: 2826

Application No.: 10/654,424

Examiner: A. Williams

Filed: September 4, 2003

Docket No.: 117031

For: WIRING BOARD HAVING INTERCONNECT PATTERN WITH LAND, AND SEMICONDUCTOR DEVICE, CIRCUIT BOARD, AND ELECTRONIC EQUIPMENT INCORPORATING THE SAME (AS AMENDED)

AMENDMENT

PROPOSED

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reply to the September 8, 2004 Office Action, please consider the following:

Amendments to the Specification;

Amendments to the Claims as reflected in the listing of claims; and

Remarks.

Amendments to the Specification

Please replace the title as follows:

WIRING BOARD HAVING INTERCONNECT PATTERN WITH LAND, AND ~~METHOD OF MANUFACTURING THE SAME,~~ SEMICONDUCTOR DEVICE, CIRCUIT BOARD, AND ELECTRONIC EQUIPMENT INCORPORATING THE SAME

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A wiring board comprising:

a substrate; ~~and~~

an interconnect pattern which is formed on the substrate and includes a ~~land,~~land having a penetration hole; and

~~wherein a penetration hole which exposes the substrate is formed in the land, and~~

~~wherein~~ a resist layer covering at least the penetration hole, the penetration hole ~~is~~ being formed in a region along a periphery of the land.

2. (Original) The wiring board as defined in claim 1, wherein a planar shape of the land is approximately circular.

3. (Currently Amended) The wiring board as defined in claim 1, wherein the penetration hole is an elongated hole exposing the substrate.

4. (Original) The wiring board as defined in claim 3, wherein the penetration hole is the elongated hole which is longer in a direction along the periphery of the land than in a direction intersecting the periphery of the land at right angles.

5. (Original) The wiring board as defined in claim 1, wherein a plurality of the penetration holes are formed in the land.

6. (Original) The wiring board as defined in claim 5, wherein the plurality of penetration holes are arranged in a region along the periphery of the land.

7. (Original) The wiring board as defined in claim 5, wherein the plurality of penetration holes are disposed so that distance between the adjacent penetration holes is approximately the same.

8. (Currently Amended) The wiring board as defined in claim 1, further comprising:

~~a~~ the resist layer ~~which is~~being formed on a surface of the substrate on which the interconnect pattern is formed and includes an opening which exposes at least a part of the land.

9. (Original) The wiring board as defined in claim 8, wherein a planar shape of the opening of the resist layer is approximately circular.

10. (Original) The wiring board as defined in claim 8, wherein the resist layer covers at least a part of the penetration hole.

11. (Original) The wiring board as defined in claim 8,

wherein the resist layer covers the penetration hole, and

wherein part of an edge of the penetration hole is in contact with an edge of the opening of the resist layer.

12. (Original) The wiring board as defined in claim 1, which is formed as an interposer.

13. (Original) The wiring board as defined in claim 1, which is formed as a motherboard.

14. (Original) A semiconductor device comprising:

the wiring board as defined in claim 1, and

a semiconductor chip which is electrically connected with the interconnect pattern.

15. (Original) The semiconductor device as defined in claim 14, further comprising an external terminal formed on the land.

16. (Original) A circuit board on which the semiconductor device as defined in claim 14 is mounted.

17. (Original) Electronic equipment comprising the semiconductor device as defined in claim 14.

18. (Withdrawn) A method of manufacturing a wiring board, comprising:

forming an interconnect pattern including a land on a substrate,

wherein a penetration hole which exposes the substrate is formed in a region along a periphery of the land.

19. (Withdrawn) The method of manufacturing a wiring board as defined in claim 18, wherein the penetration hole is formed at the same time as the interconnect pattern.

20. (Withdrawn) The method of manufacturing a wiring board as defined in claim 18, wherein a plurality of the penetration holes are formed in the land.

21. (Withdrawn) The method of manufacturing a wiring board as defined in claim 18, further comprising:

forming a resist layer on a surface of the substrate, on which the interconnect pattern is formed, in a manner that the resist layer includes an opening which exposes at least a part of the land.

REMARKS

Claims 1-21 are pending in this application. The Office Action withdraws claims 18-21 from consideration. By this Amendment, the title of the invention is amended; and claims 1, 3 and 8 are amended. No new matter is added. In view of the foregoing amendments and following remarks, reconsideration and allowance are respectfully requested.

I. The Specification Satisfies All Formal Requirements

The Office Action objects to the title of the invention. In response, the title of the invention is amended to obviate the objection. Withdrawal of the objection to the title of the invention is respectfully requested.

II. Rejection Under 35 U.S.C. §102(b)

The Office Action rejects claims 1-17 under 35 U.S.C. §102(b) over U.S. Patent No. 5,973,931 to Fukasawa. This rejection is respectfully traversed.

Fukasawa does not disclose "a resist layer covering at least the penetration hole, the penetration hole being formed in a region along a periphery of the land," as recited in claim 1. Fukasawa discloses that "in the first preferred embodiment described above a gap of over 0.05 mm is provided between the land 16 and the pattern-protecting film 17 "(col. 4, lines 41-48; Fig. 4b). As shown in Fig. 4b, the pattern forming film 17 does not cover the peripheral opening, but only partially covers the peripheral opening up to the diameter D1, leaving an uncovered gap surrounding the land 16. Accordingly, Fukasawa does not anticipate a resist layer covering at least the penetration hole, as recited in claim 1. Claim 1 is not anticipated by Fukasawa. Claims 2-17 depend from claim 1, and thus, claims 2-17 are also not anticipated by Fukasawa. Accordingly, reconsideration and withdrawal of the rejection are respectfully requested.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-21 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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